I hereby certify that this correspondence is being filed via EFS-Web with the United States Patent and Trademark Office on September 12, 2006.

TOWNSEND and TOWNSEND and CREW LLP

By: J. Matt

J. Matthew Zigmant

PATENT
Attorney Docket No.: 015114-054810US
Client Ref. No.: A00718

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of:

Yan Chong et al.

Application No.: 10/037,861

Filed: January 2, 2002

For: SELF-COMPENSATING DELAY CHAIN FOR MULTIPLE-DATE-RATE INTERFACES

Customer No.: 26059

Confirmation No. 4806

Examiner: Vincent H. Tran

Technology Center/Art Unit: 2115

AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the office action mailed April 12, 2006, please enter the following amendments and remarks:

**Amendments to the Claims** are reflected in the listing of claims which begins on page 2 of this paper.

**Remarks/Arguments** begin on page 10 of this paper.

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings of claims in the application:

**Listing of Claims:**

Claims 1-15 (Cancelled)

Claim 16. (Currently amended) ~~The integrated circuit of claim 15 further comprising:~~ An integrated circuit comprising:

a series of circuits;

a phase detector having a first input coupled to an input of the series of circuits and a second input coupled to an output of the series of circuits;

an up/down counter having an input coupled to an output of the phase detector;

a first variable-delay block having a control input coupled to an output of the up/down counter;

an input buffer;

a first register having an input coupled to an output of the input buffer and a clock input coupled to an output of the first variable-delay block;

a second register having an input coupled to the output of the input buffer and a complementary clock input coupled to the output of the first variable-delay block; and

a third ~~flip-flop~~ register coupled between the phase detector and the up/down counter,

wherein the series of circuits comprises:

a second variable-delay block having a control input coupled to the output of the up/down counter; and

a frequency divider.

Claim 17. (Currently amended) The integrated circuit of claim ~~14~~ 16 wherein an input of the second variable-delay block is coupled to an output of the frequency divider.

Claim 18. (Currently amended) The integrated circuit of claim ~~14~~ 16 wherein an output of the frequency divider is coupled to an input of the second variable-delay block.

Claim 19. (Cancelled)

Claim 20. (Currently amended) The integrated circuit of claim ~~19~~ 25 wherein the first frequency divider ~~is configured to receive~~ receives the first clock signal and the first variable-delay block ~~is configured to receive~~ receives an output from the first frequency divider.

Claim 21. (Currently amended) The integrated circuit of claim ~~19~~ 25 wherein the first variable-delay block ~~is configured to receive~~ receives the first clock signal and the first frequency divider ~~is configured to receive~~ receives an output from the first variable-delay block.

Claim 22. (Cancelled)

Claim 23. (Currently amended) The integrated circuit of claim ~~22~~ 25 further comprising:

a memory ~~configured~~ to receive an output of the first flip-flop and an output of the second flip-flop.

Claim 24. (Currently amended) The integrated circuit of claim ~~22~~ 25 further comprising:

an synchronous dynamic random access memory ~~configured~~ to receive an output of the first flip-flop and an output of the second flip-flop.

Claim 25. (Currently amended) ~~The integrated circuit of claim 22 further comprising:~~ An integrated circuit comprising:

a series combination of a first frequency divider and a first variable-delay block, to receive a first clock signal;

a phase detector to receive the first clock signal and an output from the series combination;

an up/down counter to receive an output from the phase detector;

a second variable-delay block to receive a second clock signal;

a first flip-flop having a clock input to receive an output of the second variable-delay block;

a second flip-flop having a complementary clock input to receive the output of the second variable-delay block; and

a third flip-flop coupled between the phase detector and the up/down counter,

wherein the first variable-delay block and the second variable-delay block receive an output from the up/down counter.

Claim 26. (Currently amended) The integrated circuit of claim 25 further comprising:

a second frequency divider ~~configured~~ to receive the first clock signal to provide a third clock signal to the up/down counter.

Claim 27. (Currently amended) The integrated circuit of claim ~~19~~ 25 wherein the integrated circuit is a programmable logic device.

Claim 28. (Currently amended) A computing system comprising:

a multiple-data-rate memory; and

the integrated circuit of claim ~~14~~ 16 coupled to the multiple-data-rate memory.

Claim 29. (Original) The computing system of claim 28 wherein the multiple-data-rate memory is a double-data-rate memory.

Claims 30-33. (Cancelled)

Claim 34. (Currently amended) An integrated circuit comprising:

a first input buffer having an input coupled to a first pad;

a double data rate register comprising:

a first register having a data input responsive to a signal at an output of the first input buffer and a rising-edge triggered clock input; and

a second register having a data input coupled to the data input of the first register and a falling-edge triggered clock input coupled to the rising-edge triggered clock input of the first register; ~~and~~

a delay control circuit comprising:

an up/down counter; and

a first variable delay block coupled to the up/down counter to set a delay; and

a second variable delay block separate from the first variable delay block and coupled to provide ~~a~~ the delay between a signal at the data input of the first register and a signal at the rising-edge triggered clock input of the first register.

Claim 35. (Previously Presented) The integrated circuit of claim 34 wherein a count provided by the up/down counter sets the delay between the signal at the data input of the first register and the signal at the rising-edge triggered clock input of the first register.

Claim 36. (Currently amended) The integrated circuit of claim 35 further comprising a bypass path to bypass the second variable delay element.

Claim 37. (Currently amended) The integrated circuit of claim 35 further comprising a multiplexer having a first input coupled to an input of the second variable delay element and an output coupled to an output of the second variable delay element.

Claim 38. (Previously Presented) The integrated circuit of claim 35 further comprising:

a second input buffer coupled to a second pad to receive a DQS signal,

wherein the rising-edge triggered clock input of the first register is responsive to a signal at the output of the second input buffer, and a DQ signal is received at the first pad.

Claim 39. (Previously Presented) The integrated circuit of claim 38 wherein a clock signal is used in generating the count provided by the up/down counter.

Claim 40. (Previously Presented) The integrated circuit of claim 35 further comprising:

a plurality of programmable logic elements, configurable to perform user-defined logic functions; and

a plurality of logic interconnect lines configurable to couple the plurality of programmable logic elements to the double-data rate register.

Claim 41. (Currently amended) The integrated circuit of claim 35 wherein the second variable delay block comprises a series of delay elements.

Claim 42. (Currently amended) An integrated circuit comprising:

a first input buffer having an input coupled to a first pad;

a first register having a data input responsive to a signal at an output of the first input buffer and a rising-edge triggered clock input;

a second register having a data input coupled to the data input of the first register and a falling-edge triggered clock input coupled to the rising-edge triggered clock input of the first register; ~~and~~

a delay control circuit comprising:

a control circuit including an up/down counter; and

a first variable delay circuit coupled to the up/down counter to adjust a variable delay;

a second variable delay circuit separate from the first variable delay circuit and coupled to provide ~~a~~ the variable delay between a signal at the data input of the first register and a signal at the rising-edge triggered clock input of the first register; and

a multiplexer having a first input coupled to an input of the second variable delay circuit and a second input coupled to an output of the second variable delay circuit.

Claim 43. (Currently amended) The integrated circuit of claim 42 wherein the up/down counter provides a count to the second variable delay circuit, and wherein the count determines the delay between the signal at the data input of the first register and the signal at the rising-edge triggered clock input of the first register.

Claim 44. (Currently amended) The integrated circuit of claim 43 wherein the multiplexer provides a bypass path for bypassing the second variable delay circuit.

Claim 45. (Previously Presented) The integrated circuit of claim 43 further comprising:

a second input buffer coupled to a second pad to receive a DQS signal,

wherein the rising-edge triggered clock input of the first register is responsive to a signal at the output of the second input buffer, and a DQ signal is received at the first pad.

Claim 46. (Previously Presented) The integrated circuit of claim 45 wherein a clock signal is used in generating the count provided by the up/down counter.

Claim 47. (Previously Presented) The integrated circuit of claim 43 further comprising:

a plurality of programmable logic elements, configurable to perform user-defined logic functions; and

a plurality of logic interconnect lines configurable to couple the plurality of programmable logic elements to the first register and the second register.

Claim 48. (Previously Presented) The integrated circuit of claim 43 wherein the integrated circuit is a field programmable gate array.

Claim 49. (Currently amended) The integrated circuit of claim 43 wherein the second variable delay circuit comprises a series of delay elements.

Claim 50. (Currently amended) An integrated circuit comprising:

a rising-edge triggered register having a data input and a clock input;

a falling-edge triggered register having a data input coupled to the data input of the rising-edge triggered register and a clock input coupled to the clock input of the rising-edge triggered register;

a first series of delay circuits coupled to provide a variable delay between a signal at the data input and a signal at the clock input of the first register;

a multiplexer having an input coupled to an input of the first series of delay circuits and an output coupled to an output of the first series of delay circuits; ~~and~~

a counter having an output coupled to the first series of delay circuits; and

a second series of delay circuits distinct from the first series of delay circuits and coupled the counter to adjust the variable delay.

Claim 51. (Currently amended) The integrated circuit of claim 50 wherein the counter provides a count to the first and second series of delay circuits;

wherein the count is incremented and decremented to vary the variable delay.

Claim 52. (Currently amended) The integrated circuit of claim 50 wherein the multiplexer provides a bypass path for bypassing the first series of delay circuits.

Claim 53. (Currently amended) The integrated circuit of claim 50 further comprising:

~~a second~~ an input buffer coupled to a second pad to receive a DQS signal,

wherein the clock input of the rising-edge triggered register is responsive to a signal at the output of the ~~second~~ input buffer, and a DQ signal is received at the first pad.

Claim 54. (Previously Presented) The integrated circuit of claim 50 wherein a clock signal is used in generating the count provided by the counter.

Claim 55. (Previously Presented) The integrated circuit of claim 50 further comprising:

a plurality of programmable logic elements, configurable to perform user-defined logic functions; and

a plurality of logic interconnect lines configurable to couple the plurality of programmable logic elements to the rising-edge triggered register and the falling edge-triggered register.

Claim 56. (Previously Presented) The integrated circuit of claim 50 wherein an output of the rising-edge triggered register is coupled to a first-in-first-out memory.

## REMARKS/ARGUMENTS

After entry of this amendment, claims 16-18, 20-21, 23-29, and 34-56 will remain pending in this application. Claims 20, 21, 23, 24, 26, 34, 42, and 50 have been amended. Claims 36, 37, 41, 43, 44, 49, 51, and 52 have been amended for consistency. Claims 16 and 25 have been rewritten as independent claims. The dependencies of claims 17, 18, 20, 21, 23, 24, 27, and 28 have been appropriately amended. Claim 53 has been amended to correct a typographical oversight. Claims 14-15, 19, 22, and 30-33 have been cancelled. Support for the amended claims can be found in the specification. No new matter has been added.

Claims 48 and 53 stand rejected under 35 U.S.C. 112 second paragraph. Claim 14 stands rejected under 35 U.S.C. 102(b) as being anticipated by Funaba, United States patent number 6,212,127. Claims 34-35 stand rejected under 35 U.S.C. 102(e) as being anticipated by Vogt et al., United States patent number 6,316,980. Claims 14-15, 19, 21-24, 27-33 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagawa, United States patent application number 20010046163 in view of Kobayashi et al., United States patent number 6,509,776. Claims 17-18 and 20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagawa and Kobayashi in further view of Fiscus, United States patent number 6,492,852. Claims 34-50 and 53 stand rejected under 35 U.S.C. 102(b) as being unpatentable over McCracken et al., United States patent number 6,279,073 in view of Murakami, United States patent application number 20010004335 and Vogt. Reconsideration of these rejections in light of these amendments and remarks is respectfully requested.

35 U.S.C. 112 rejections

Claim 48 stands rejected under 35 U.S.C. 112 second paragraph. Specifically, the pending office action states that claim 48 recites a "filed programmable gate array." (See pending office action, page 2, paragraph 2.)

Claim 48 of the amendment filed February 6, 2006 correctly recites a "field programmable gate array." No claim could be found that recites a "filed programmable gate array." Withdrawal or clarification of this rejection is respectfully requested.

Claim 53 also stands rejected under 35 U.S.C. 112 second paragraph. Claim 53 has been amended appropriately.

Claim 34

Claim 34 stands rejected under 35 U.S.C. 102(b) as being anticipated by Vogt. But Vogt does not teach each and every element of this claim. For example, claim 34, as amended, recites "a first variable delay block coupled to the up/down counter to set a delay; and a second variable delay block separate from the first variable delay block and coupled to provide the delay between a signal at the data input of the first register and a signal at the rising-edge triggered clock input of the first register." Vogt does not provide this feature.

The pending office action cites Figure 2 of Vogt as teaching each and every element of this claim. (See pending office action, page 3, paragraph 8.) But Figure 2 of Vogt does not provide a second delay block as required by the claim.

Rather, Figure 2 of Vogt teaches a circuit having several delay elements that are coupled in series when a delay is set or calibrated. (See Vogt, column 3, lines 51-54.) The individual delay elements are then used to delay strobe signals during device operation. (See Vogt, column 3, lines 47-50.) Thus, Vogt uses the same delay elements to set a delay and to delay a strobe signal. Thus, Vogt does not provide a second delay block separate from the first delay block as required by the claim.

Claim 34 also stands rejected under 35 U.S.C. 102(b) as being unpatentable over McCracken in view of Murakami and Vogt. But these additional references do not provide the required second delay block either. For example, Figure 3 of McCracken provides a single delay line for each strobe signal provided by an SDRAM. (See McCracken, Figure 3.)

For at least these reasons, claim 34 should be allowed.

Other claims

Claims 42 and 50 should be allowed for similar reasons as claim 34. Claims 16 and 25 have indicated as being allowable if written in independent form. Accordingly, claims 16 and 25 have been rewritten in independent form. The other claims depend on one of the above

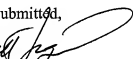
claims and should be allowed for at least the same reasons and for the additional limitations they recite.

## CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this application are in condition for allowance. The issuance of a formal notice of allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



J. Matthew Zigmant
Reg. No. 44,005

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 415-576-0200
Fax: 415-576-0300
Attachments
JMZ:deb
60823641 v1